base region **1907** and p-type well region **1906** below gate electrode **1912**. Electrons flow from cathode region **1933** to n-type base region **1908** via the inversion layer. The electrons are injected into p-type anode region **1934**. This electron current functions as a base current of a pnp transistor consisting of p-type anode region **1934**, n-type buffer region **1909** and n-type base region **1908**, and p-type base region **1907**. The base current turns on the transistor, thereby causing conductivity modulation to occur. As a result of this conductivity modulation, a large current flows between terminals A and K.

Applying a negative voltage, higher than a threshold value, across gate electrode **1912** and cathode electrode **1935**, creates an inversion layer in a surface layer of n-type cathode region **1933** below gate electrode **1912**. Since p-type cathode region **1937** is connected via the inversion layer to p-type base region **1907** while n-type cathode region **1933** is disconnected, electrons are not fed to n-type base region **1908**. The transistor therefore turns off, interrupting the current flow between the terminals A and K.

Since n-type well region **1903** is electrically connected to p-type anode region **1934** via n-type contact region **1916**, a parasitic pnp transistor with p-type substrate **1901** as its collector remains off. Therefore, the foregoing problems of the prior art are avoided. The device of FIG. **19** greatly lowers switching loss as does the first embodiment.

N-type buffer region **1909** is optionally omitted in some cases. The n-type well region is optionally replaced by an epitaxial layer. An auxiliary electrode **1919** on n-type contact region **1916** is optionally not connected to anode electrode **1936**, similar to the IGBT of the second embodiment, to bias auxiliary electrode **1919** at a high potential. Alternatively, auxiliary electrode **1919** is not disposed, thereby floating the potential of the n-type semiconductor region outside the p-type well region. These modifications neither change the operations of the LMCT's nor impair their merits.

Though the above embodiments are explained by way of n-channel LMCT's, it is apparent to one skilled in the art that the structures of the invention are applicable to p-channel LMCT's, including semiconductor regions of opposite conductivity type to those of the n-channel LMCT's.

The LMCT's of FIGS. **20–23** function similarly, thereby greatly reducing switching loss.

Twentieth Embodiment

Referring to FIG. **20**, an LMCT according to a twentieth embodiment is shown. Since the twentieth through twenty-third embodiments are a modification of the nineteenth embodiment, discussion of the structural similarities is omitted. An n-type base region **2008** in a surface portion of a p-type well region **2006** is made large enough to contain a p-type base region **2007**. N-type base region **2008**, which contains a part of p-type base region **2007** in FIG. **20**, is optionally extended to completely contain p-type base region **2007**.

Twenty-first Embodiment

Referring to FIG. **21**, an LMCT according to a twenty-first embodiment is shown. A p-type well region **2106** contains a p-type base region **2107**. An n-type base region **2108** is formed partly in a surface portion of p-type base region **2107** and partly in a surface portion of p-type well region **2106**. An n-type cathode region **2133** in a portion of p-type base region **2107** contains a p-type cathode region **2137**. Since p-type well region **2106** doesn't extend between n-type base region **2108** and p-type cathode region **2137**, a gate electrode **2112** is only above n-type cathode region **2133** and p-type base region **2107**.

Twenty-second Embodiment

Referring to FIG. **22**, an LMCT according to a twenty-second embodiment is shown in which a p-type base region (reference numeral **2107** in FIG. **21**) is omitted. Alternatively, this embodiment may be considered as having a virtual p-type base region so large as to completely contain an n-type base region **2108** and to overlap a p-type well **2206**. A gate electrode **2212** is above an n-type cathode region **2233** and a p-type well region **2206**.

Twenty-third Embodiment

Referring to FIG. **23**, an LMCT according to a twenty-third embodiment is shown in which a p-type base region **2307** is formed so as to contain an n-type base region **2308** but not to contain an n-type cathode region **2333**. A gate electrode **2312** is above n-type cathode region **2333**, p-type well region **2306**, and p-type base region **2307**.

Having described preferred embodiments of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications may be effected therein by one skilled in the art without departing from the scope or spirit of the invention as defined in the appended claims.

What is claimed is:

1. A lateral semiconductor arrangement comprising:

a semiconductor substrate of a first conductivity type;

a first semiconductor region of a second conductivity type on said semiconductor substrate;

a semiconductor device;

said semiconductor device including a well region of said first conductivity type in a surface portion of said first semiconductor region;

a second region of said second conductivity type being more heavily doped than said first region of said second conductivity type;

said second region being positioned between said first region and said semiconductor substrate and being effective to prevent punch-through between said well region and said semiconductor substrate;

a first main electrode on said well region;

a second main electrode on said well region;

a control electrode disposed above said well region;

a first electrode region of said first conductivity tape making contact with said first main electrode;

a buffer region of said second conductivity type surrounding said first electrode region;

a third region of said second conductivity type beneath said buffer region; and

said buffer region being doped more heavily than said second region.

2. A lateral semiconductor arrangement according to claim **1**, further comprising an auxiliary electrode on said first semiconductor region of said second conductivity type.

3. A lateral semiconductor arrangement according to claim **2**, wherein said first main electrode is electrically connected to said auxiliary electrode.

4. A lateral semiconductor arrangement according to claim **1**, further comprising an auxiliary electrode on said second region of said second conductivity type.